AMENDMENT TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

Claims 1 to 27. (Canceled).

28. (Currently Amended) An instruction pipeline in a microprocessor, comprising:

a plurality of pipeline units, each of the pipeline units configured to process instructions, at least one of the plurality of pipeline units configured to receive the instructions from another of the pipeline units and store the instructions, wherein the instructions are distributed in multiple threads for the plurality of pipeline units to process[[,]] and the at least one of the plurality of pipeline units is configured to reissue to a downstream pipeline unit at least one of the instructions in one of the multiple threads after a stall occurs in the one of the multiple threads, the reissued at least one of the instructions having been previously issued to the downstream pipeline unit.

29. (Currently Amended) An instruction pipeline in a microprocessor, comprising:

at least one upstream pipeline unit configured to issue each of a series of instructions on one of a plurality of instruction threads;

at least one downstream pipeline unit configured to allocate each of the series of instructions on the one of the plurality of instruction threads on which each of the series of instructions were issued; and

an instruction queue, wherein in a first operating mode, the instruction queue being configured to pass each of the series of instructions ~~instruction~~ from the at least one upstream pipeline unit to the at least one downstream pipeline unit on the one of the plurality of instruction threads on which each of the series of instructions were issued and configured to store each of the series of instructions, at least one memory location being dedicated to each of the plurality of instruction threads, and in a second operating mode the instruction queue configured to reissue to the at least one downstream pipeline unit at least one of the series of instructions on the one of the plurality of instruction threads on which the at least one of the series of instructions was issued.

30. (Previously Presented) The instruction pipeline of claim 29, wherein the instruction queue in the first operating mode is configured to alternate passing the series of instructions on the one of the plurality of instruction threads on which each of the series of instructions were issued when a stall signal is not present on any of the plurality of instruction threads, and when the stall signal is present on one of the plurality of instruction threads, the instruction queue is configured to issue the series of instructions on an other one of the plurality of instruction threads.

31. (Previously Presented) The instruction pipeline of claim 29, wherein the at least one upstream pipeline unit is configured to determine the one of the plurality of instruction threads on which to issue each of the series of instructions based the availability of resources on each of the plurality of instruction threads.

32. (Currently Amended) [[An]] A method of processing instructions in a multi-threaded instruction pipeline, comprising:

issuing, from an upstream pipeline unit, instructions on one of a plurality of instruction threads;

storing the issued instructions in a queue, and passing the issued instructions to a downstream unit on the one of the plurality of instruction threads;

detecting a stall in the one of the plurality of instruction threads; and

after detecting the stall, reissuing at least one of the issued instructions from the queue, on the one of the plurality of instruction threads on which the instructions were issued.

33. (Previously Presented) The method according to claim 32, further comprising:

maintaining a respective pointer for each of the plurality of instruction threads, wherein the reissuing step includes reissuing the at least one of the issued instruction from the queue using the respective pointer for the one of the plurality of instruction threads on which the instruction was issued.

34. (Previously Presented) The method according to claim 32, further comprising:

alternating the issuance of instructions between each of the plurality of instruction threads.

35. (Currently Amended) The method according to claim 32, further comprising:

selecting one of the plurality of ~~instructing~~ instruction threads on which to issue the instructions based on an availability of resources.

36. (Currently Amended) A microprocessor, comprising:

a multi-threaded instruction pipeline including at least one upstream pipeline unit configured to issue instructions on a selected one of a plurality of threads of the pipeline, an instruction queue configured to pass issued instructions to a downstream pipeline unit on the selected one of the plurality of threads and store a copy of the issued instructions, the instruction queue further configured to reissue, on the selected one of the plurality of threads, at least one of the stored instructions ~~instruction~~ in an event of a downstream stall on the selected one of the plurality of threads.

37. (Previously Presented) The microprocessor according to claim 36, wherein the at least one upstream pipeline unit includes at least one of a trace cache and a micro-instruction sequencer.

38. (Previously Presented) The microprocessor according to claim 36, wherein the downstream pipeline unit includes an execution unit.

39. (Previously Presented) The microprocessor according to claim 36, wherein the instruction queue is configured to select one of the threads based on available resources.

40. (Previously Presented) The microprocessor according to claim 36, wherein the instruction queue is configured to alternate between the plurality of threads when passing the instructions.

41. (Previously Presented) The microprocessor according to claim 36, wherein the instruction queue is configured to pass instructions on one of the threads, and configured to switch to a different one of the threads when a stall is detected on the one of the threads.

42. (Previously Presented) The microprocessor according to claim 36, wherein the instruction queue includes:

a memory device to store the instructions; and

an output multiplexer which is configured, in a first mode of operation, to pass instructions from the upstream pipeline unit to the downstream pipeline unit, and which is configured, in a second mode of operation, to reissue the at least one of the stored instructions.